CLAIMS

What is claimed is:

1. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

a test bench external bus interface unit (EBIU) connected to said verification interface model,

wherein said test bench EBIU is connected to a SOC EBIU within said SOC.

2. The verification test bench system in claim 1, wherein said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model.

3. The verification test bench system in claim 1, wherein said SOC interface and said verification interface model are programmed by a test case running in said SOC.

4. The verification test bench in claim 3, wherein said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

5. The verification test bench in claim 3, wherein said test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

6. The verification test bench system in claim 1, wherein said verification interface model tests an operational capability of said SOC interface.

7. The verification test bench system in claim 1, further comprising at least one additional verification interface model connected to said test bench EBIU for testing additional types of SOC interfaces.

8. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

a test bench external bus interface unit (EBIU) connected to said verification interface model,

wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and

wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in said SOC.

9. The verification test bench system in claim 8, wherein said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model.

10. The verification test bench system in claim 8, wherein said SOC interface and said verification interface model are programmed by the same test case running in said SOC.

11. The verification test bench in claim 10, wherein said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

12. The verification test bench in claim 10, wherein said test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

13. The verification test bench system in claim 8, wherein said verification interface model tests an operational capability of said SOC interface.

14. The verification test bench system in claim 8, further comprising at least one additional verification interface model connected to said test bench EBIU for testing additional types of SOC interfaces.

15. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

a test bench external bus interface unit (EBIU) connected to said verification interface model,

wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and

wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in said SOC, such that said SOC interface and said verification interface model are programmed by the same test case running in said SOC.

16. The verification test bench system in claim 15, wherein said SOC EBIU allows said test case to control both said SOC interface and said verification interface model.

17. The verification test bench in claim 15, wherein said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

18. The verification test bench in claim 15, wherein said test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

19. The verification test bench system in claim 15, wherein said verification interface model tests an operational capability of said SOC interface.

20. The verification test bench system in claim 15, further comprising at least one additional verification interface model connected to said test bench EBIU for testing additional types of SOC interfaces.

21. A method of testing a system-on-a-chip (SOC) interface of an SOC, said method comprising:

connecting a verification interface model to said SOC interface;

connecting a test bench external bus interface unit (EBIU) to said verification interface model;

connecting said test bench EBIU to a SOC EBIU within said SOC; and

comparing said SOC interface with said interface model.

22. The method in claim 21, further comprising allowing, through said SOC EBIU, a test case running in said SOC to control both said SOC interface and said verification interface model.

23. The method in claim 21, further comprising programming said SOC interface and said verification interface model by a test case running in said SOC.

24. The method in claim 23, wherein said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

25. The method in claim 23, wherein said test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

26. The method in claim 21, wherein said comparing process tests an operational capability of said SOC interface.

27. The method in claim 21, further comprising:

connecting at least one additional verification interface model to said test bench EBIU; and

testing additional types of SOC interfaces.

28. A program storage device readable by machine tangibly embodying a program of instructions executable by the machine to perform a method for testing a system-on-a-chip (SOC) interface of an SOC, said method comprising:

connecting a verification interface model to said SOC interface;

connecting a test bench external bus interface unit (EBIU) to said verification interface model;

connecting said test bench EBIU to a SOC EBIU within said SOC; and

comparing said SOC interface with said interface model.

29. The program storage device in claim 28, wherein said method further comprises allowing, through said SOC EBIU, a test case running in said SOC to control both said SOC interface and said verification interface model.

30. The program storage device in claim 28, wherein said method further comprises programming said SOC interface and said verification interface model by a test case running in said SOC.

31. The program storage device in claim 30, wherein said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

32. The program storage device in claim 30, wherein said test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

33. The program storage device in claim 28, wherein said comparing process tests an operational capability of said SOC interface.

34. The program storage device in claim 28, wherein said method further comprises:

connecting at least one additional verification interface model to said test bench EBIU; and

testing additional types of SOC interfaces.